What is claimed is:

1. A line selector for a matrix of memory elements, comprising

a plurality of matrix line group selection circuits, each one allowing the selection of a respective group of lines according to a first address, each line group including at least one matrix line,

characterized by comprising

flag means associated with each line group, that can be set to declare a pending status of a prescribed operation to be conducted on the respective line group, and

means for entrusting the flag means with the selection of the respective line group during the execution of the prescribed operation, in alternative to the respective line group selection circuit, the flag means enabling, when set, the execution of the prescribed operation on the respective line group.

2. The line selector according to claim 1, in which the matrix lines are word lines.

3. The line selector according to claim 2, in which the prescribed operation is an erase operation of the memory elements.

4. The line selector according to claim 3, in which the flag means are reset after the respective word line group has been erased.

5. The line selector according to claim 4, in which the flag means are reset after the respective word line group has passed an erase verify operation.

6. The line selector according to claim 5, further comprising setting means and resetting means, associated with each flag means for setting and, respectively, resetting the associated flag means, the setting means and resetting means being enabled by the respective line group selection circuit according to the first address.

7. The word line selector according to claim 2, in which the flag means comprises a set-reset flip-flop.

8. The line selector according to claim 2, in which the means for entrusting the flag means with the selection of the respective line group during the execution of the prescribed operation comprise means for disconnecting the line

group selection circuit from a respective line group selection signal line, and means for transferring onto the line group selection signal line a state corresponding to that of the respective flag means.

9. The line selector according to claim 2, further comprising a plurality of word line selection circuits, each one associated with a respective line group selection circuit for allowing the selection of at least one word line within a respective group of word lines, according to a second address, the word line selection circuits comprising word line driver circuits for driving potentials of the word lines.

10. The line selector according to claim 9, in which a word line driver reset circuit is associated with each line group selection circuit, activatable for resetting the word line driver circuits of the associated word line selection circuit.

11. The line selector according to claim 10, in which the word line driver reset circuit, when activated, resets the word line driver circuits of the associated word line selection circuit only if the respective group of word lines is selected.

12. A method of conducting a prescribed operation on a matrix of memory elements, comprising:

providing a line selector having a plurality of line group selection circuits, each one allowing the selection of a respective group of matrix lines according to an address, each matrix line group including at least one matrix line,

characterized by comprising

associating with each matrix line group a respective flag,

selectively setting at least one flag, to declare a pending status of the prescribed operation for the respective matrix line group, and

entrusting the flags with the selection of the respective matrix line group, as an alternative to the respective line group selection circuit, the at least one set flag enabling the execution of the prescribed operation on the respective matrix line group.

13. The method according to claim 12, in which the matrix lines are word lines.

14. The method according to claim 13, in which the prescribed operation is an erase operation.

15. The method according to claim 14, in which the setting of the at least one flag comprises selecting the matrix group via the respective line group selection circuit.

16. The method according to claim 15, further comprising applying at least one erase pulse.

17. The method according to claim 16, further comprising verifying an outcome of the at least one erase pulse by accessing the word lines in the word line group associated with the at least one set flag.

18. The method according to claim 17, in which the verifying further comprises resetting the at least one set flag if the outcome of the at least one erase pulse is positive.

19. The method according to claim 18, in which the resetting the at least one set flag further comprises selecting the associated word line group via the respective line group selection circuit.

20. The method according to claim 19, further comprising applying additional erase pulses and verifying the outcome of each additional erase pulse, until the at least one set flag is reset.

21. A memory comprising a matrix of memory elements and a line selector for selecting lines of the matrix,

characterized in that

the line selector is realised according to claim 1.

22. A line selection circuit for selecting a group of lines of an array of memory cells, the circuit comprising:

a selection circuit operable to select a group of memory cells from the array for an operation; and

a status circuit coupled to the selection circuit and operable to enable the selection circuit to perform the operation on a subset of the group of selected memory cells.

23. The line selector circuit of claim 22 wherein the selection circuit further comprises:

a row address selection circuit operable to select a row of memory cells based upon a first address signal; and

a column address selection circuit operable to select a column of memory cells based upon a second address signal.

24. The line selector circuit of claim 22 wherein the status circuit further comprises:

a logic circuit operable to store a logic state corresponding to the pending status of the operation to be performed on the selected group of memory cells; and

a circuit operable to set the state of the logic circuit based upon the previous state of the logic circuit.

25. The line selector circuit of claim 22, further comprising a resetting circuit operable to reset the status circuit to a finished state after the operation performed on the subset of the group of selected memory cells has been verified.

26. The line selector circuit of claim 22, further comprising a setting circuit operable to set the status circuit to a beginning state prior to the operation to be performed on the subset of the group of selected memory cells.

27. The line selector circuit of claim 22 wherein the group of memory cells comprises a word line.

28. A memory, comprising:

a line selector circuit including:

a selection circuit operable to select a group of memory cells from the array for an operation; and

a status circuit coupled to the selection circuit and operable to enable the selection circuit to perform the operation on a subset of the group of selected memory cells.

29. The memory of claim 28 wherein the memory comprises an electronic erasable and programmable memory.

30. An electronic system, comprising:

a memory including:

a line selector circuit having:

a selection circuit operable to select a group of memory cells from the array for an operation; and

a status circuit coupled to the selection circuit and operable to enable the selection circuit to perform the operation on a subset of the group of selected memory cells.

31. The electronic system of claim 30 wherein the memory comprises an electronic erasable and programmable memory.

32. A method comprising:

selecting a group of memory elements from an array of memory elements for an operation;

selecting a subset of the group of memory elements based upon the status of a flag element associated with the memory elements; and

performing the operation on the subset of the group of memory elements.

33. The method of claim 32 wherein the selecting of the group further comprises:

selecting a row of memory elements from the matrix of memory elements based upon a first address signal; and

selecting a column of memory elements from the array based upon a second address signal.

34. The method of claim 32 wherein the selecting of the group further comprises setting the status of the flag element to a first status.

35. The method of claim 32 wherein the selecting of the subset further comprises:

determining the status of the flag element associated with each memory element; and

selecting each memory element having a flag element with a first status.

36. The method of claim 35, further comprising

verifying the operation of the operation on each selected memory element;

setting the status of the flag element to a second status if the operation on the memory element is verified; and

performing the operation a second time if the operation on the memory element is not verified.

37. The method of claim 32 wherein the operation comprises an erase operation.